Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendments, claims 1 and 11-27 are pending in the application, with 1, 11 and 12 being the independent claims. Claims 2-10 are sought to be cancelled without prejudice to or disclaimer of the subject matter therein. New claims 14-27 are sought to be added. These changes introduce no new matter, and their entry is respectfully requested.

Based on the above amendments and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Objections to the Claims

The Examiner objected to claim 1 because the phrase "phase look loop circuit" is not consistent with the term used in the specification. Claim 1 has been amended such that the phrase no longer appears in the claim.

The Examiner objected to claim 8 because the phrase "wherein said" is disclosed twice in the claim. Claim 8 has been cancelled.

Accordingly, as all of the stated grounds of objection have been rendered moot, the Applicant respectfully requests that the objections to claims 1 and 8 be reconsidered and withdrawn.

Rejections under 35 U.S.C. § 102

The Examiner rejected original claims 1, 2, and 6 as allegedly being anticipated by Simmonds (U.S. patent 6,646,645 B2 issued on November 11, 2003) ("Simmonds, et. al."). On page 3 of the Office Action, the Examiner states that Simmonds teaches:

> "means ("Sync Card 100" for "PC 50B") for synchronizing said first and second image data [fig. 5], said synchronizing means comprising a phase lock loop circuit ("PLL 130") having a digital rate controller to control a lock rate of said phase lock loop circuit (the output of "PLL 130" is determined based on the inputted clock value) [col. 8 lines 36-56]."

The Applicants respectfully traverse this rejection.

The Applicants first provide grounds to traverse this rejection as directed towards *original* claim 1. The Applicants then respectfully submit that the same grounds for traversing the rejection remain applicable to supporting the patentability of claim 1, *as currently amended*, over Simmonds et al.

Original dependent claims 2 and 6 have been cancelled. However, Applicants acknowledge that new dependent claims 14-29 may recite combinations of elements substantially similar to those recited in original claims 2 and 6. Applicants respectfully submit, however, that such combinations are not anticipated by the Simmonds et al. because Simmonds does not teach or suggest all elements of amended independent claim 1, as discussed further below.

35 U.S.C. § 102 Rejection and Original Claim 1

Original claim 1 of the current application recited the following:

> 1. An image display system for synchronizing the display of images on a plurality of display devices, comprising:
>
> a first computer system generating a first signal representing first image data to be displayed on a first display device;

> a second computer system generating a second signal representing second image data to be displayed on a second display device; and
>
> means for synchronizing said first and second image data, said synchronizing means *comprising a phase lock loop circuit having a digital rate controller to control a lock rate of said phase [lock] loop circuit.*

The synchronization means of the current invention uses a master sync signal to synchronize the first and second image data. Regarding either the first and/or second image data, an output video clock signal is generated, wherein the video clock signal is synchronized to the master sync signal. Finally, the presentation of the (first and/or second) image data is controlled by the output video clock signal.

Within a single computer responsible for the first or second image, the phase locked loop (PLL) of the present invention serves at least two purposes: First, the PLL generates the video clock signal that is synchronized with the input master sync signal; second, in the event that the video clock signal loses synchronization with the input master sync signal, the PLL reestablishes the synchronization between the video clock signal and the master sync signal.

> "Phase detector 304, LPF 306 and VCO 308 are elements of a conventional phase-locked loop (PLL)." (See page 7, paragraph 31 of the present application)
>
> "The resultant loop of the invention produces a stable video clock signal 309 that is synchronized with the master sync signal." (See page 9, paragraph 38 of the present application)

Further regarding the current invention, where the "digital rate controller" controls a "lock rate of said phase lock loop circuit", the lock rate determines the duration in time over which the PLL reestablishes synchronization between the video clock signal and the master sync signal. A faster lock rate results in a shorter duration in time for the resynchronization to be effected, and a slower lock rate results in a longer

duration in time for the resynchronization to be effected. For example, page 4, paragraph 15 of the present application teaches:

> "Another aspect of the invention is the phase-locked loop circuit having a digital rate controller. The digital rate control feature allows the phase-locked loop to be programmable so that its speed can be adjusted to react more quickly or more slowly to changes."

Similarly, page 8, paragraph 35 of the present application teaches:

> "In one embodiment, rate controller 316 [part of the digital rate controller 314] includes a programmable register.... Rate controller 316 may be programmed by placing in the register the programmable lock speed (i.e., a value that will control how fast or slow the phase-locked loop will respond to changes in the master sync signal).... [The] rate controller 316... control[s] the speed or responsiveness of the phase-locked loop. The result is a loop that reacts quickly, but does not introduce jitter or other visual distortions or artifacts into the video signal."

Thus, the claimed synchronization means of the present invention comprising, "*a phase lock loop circuit having a digital rate controller to control a lock rate of said phase lock loop circuit*", refers to a means ("phase-lock loop circuit") to keep an output video clock signal synchronized with an input master sync signal; and also refers to a means ("digital rate controller") to determine how fast or how slowly (the "lock rate") the input signal and the output signal are resynchronized (i.e., put back in "lock").

Applicants respectfully point out that Simmonds does not disclose or suggest the same features as the Applicant's invention. In col. 8, lines 36-56 (the text cited by the Examiner), Simmonds, et. al. discloses:

> "FIG. 5 is a block diagram of the *sync card 100 employing an automatic master/slave detection mechanism such that the sync card 100 can automatically determine if it is a master or a slave using a LOCK output 134 of a phase lock loop (PLL) 130.* In particular, the PLL 130 receives as input the external reference clock 104 as well as one of the clock outputs 132, e.g., Q0 clock output, connected via a feedback loop. *The multiplexer 122 then, based on the LOCK*

> *output of the PLL 134, selects either the reference clock generated by the internal reference clock oscillator 120 where the sync card 100 is a master,* i.e., where the LOCK fails, *or the external reference clock input 104 where the sync card 100 is a slave*, i.e., where the LOCK succeeds."
>
> "Thus, a multi-chassis system employing sync cards such an automatic master/slave detection mechanism is self-configuring, dependent only upon cable connections. It is noted that, *although the use of a PLL is preferred, any other master/slave detection mechanism may be implemented.* For example, a switch may be alternatively used or a single master and one or more slave sync cards may be expressly incorporated into the circuit design."

Here it is clearly disclosed that the PLL is used to select between "the internal reference clock oscillator" or "the external reference clock input". The LOCK of the PLL determines whether the sync card is a master or slave device, that is, whether the sync card utilizes an internal oscillator or an external oscillator. Put another way, the PLL of Simmonds et al. selects between an internal and an external oscillator. This is stated again elsewhere in Simmonds, et. al., at col. 4, lines 13-28:

> "Each sync card preferably comprises a reference clock oscillator for generating an internal reference clock source, an external reference clock input from a previous sync card corresponding to a previous chassis, if any, and *a multiplexer for selecting the internal reference clock source where the sync card is a master and the external reference clock input where the sync card is a slave.*"
>
> "In one preferred embodiment, the sync card further *comprises a phase lock loop (PLL) for automatic determination of whether the sync card is a master or slave.* The PLL receives as input the external reference clock input and a clock output of the PLL connected via a feedback loop. The multiplexer receives an output of the PLL as in put [sic] and selects the internal reference clock source if the PLL fails to lock and the external reference clock input if the PLL locks."

In other words, in Simmonds, et. al., the PLL, in conjunction with a multiplexer, determines whether the sync card is a master device which uses its own reference clock, or whether the sync card relies on an external reference clock input.

Nowhere in Simmonds, et. al., is there either a disclosure or suggestion of any means to ensure that an output video signal, generated by either a PLL or by other means, *remains synchronized* with the external reference clock input. As such, neither does Simmonds, et. al., disclose or suggest a digital rate controller or analogous means to determine a "lock rate" of convergence between an external reference signal and an output video signal. Consequently, Simmonds, et. al. does not disclose a " *phase lock loop circuit having a digital rate controller to control a lock rate of said phase lock loop circuit*".

For the reasons cited above, Applicants respectfully submit that Simmonds, et. al., does not anticipate *original* claim 1 because it does not teach or suggest each and every feature of that claim.

35 U.S.C. § 102 Rejection and Currently Amended Claim 1

Applicants have amended claim 1 to read as follows:

1. (*currently amended*) An image display system for synchronizing the display of images on a plurality of display devices, comprising:
a first computer system generating a first signal representing first image data to be displayed on a first display device;
a second computer system generating a second signal representing second image data to be displayed on a second display device; and
means for synchronizing said first and second image data, said synchronizing means comprising:
a master sync signal generated from a master sync signal generator;
a signal generating means for receiving the master sync signal and generating a video clock signal from the master sync signal wherein the video clock signal is synchronized with the master sync signal;
wherein if the video clock signal is no longer synchronized with the master sync signal, the signal generating means reestablishes the synchronization between the video clock signal and the master sync signal; and
wherein the reestablishment of the synchronization between the video clock signal and the master sync signal occurs over a convergence time, wherein the duration of the convergence time is programmable.

Amended claim 1 no longer makes reference to the PLL or the digital rate controller, both of which are instead recited in new dependent claim 14. However, amended claim 1 recites the functionality presented in original claim 1, as well as reciting elements of the invention previously included in some of the cancelled dependent claims 2-10.

In particular, amended claim 1 recites that the signal generating means "reestablishes the synchronization between the master sync signal and the video clock signal" in the event that the synchronization is lost, and that "the reestablishment of the synchronization occurs over a convergence time, wherein the duration of the convergence time is programmable."

Applicants submit that the language of amended claim 1 at least embodies the functionality of original claim 1, wherein it was recited that the I/O module employs a "synchronizing means", and that the synchronizing means comprises "a phase lock loop circuit having a digital rate controller to control a lock rate of said phase lock loop circuit".

Specifically:

- Amended claim 1 recites that the signal generating means "reestablishes the synchronization between the master sync signal and the video clock signal"; the reestablishment is done via the "phase lock loop circuit" which was recited in original claim 1.
- Amended claim 1 recites that the signal generating means controls a "duration of the convergence time"; the duration is determined by the "lock rate" recited in original claim 1.
- Amended claim 1 recites that "the duration of the convergence time is *programmable*"; the means for this programming is the "digital rate controller" recited in original claim 1: "a digital rate controller to control a lock rate of said phase lock loop..."

Applicants submit that as the language of amended claim 1 at least encompasses the functionality of original claim 1; and further, that as original claim 1 is not anticipated by Simmonds et al., as discussed above; that therefore the features of the present invention as recited in amended claim 1 are fully patentable over Simmonds et al.

Specifically, Applicants submit that nowhere in Simmonds et. al., is there either a teaching or suggestion of any means to ensure that an output video signal, generated by either a PLL or by other means, can *reestablish synchronization* with the external reference clock input (i.e., the master sync signal). As such, neither does Simmonds, et. al., teach or suggest a means to determine a convergence time between the external reference signal and an output video signal. Consequently, Simmonds et. al. does not disclose that "*the signal generating means reestablishes the synchronization between the master sync signal and the video clock signal; and wherein the reestablishment of the synchronization occurs over a convergence time, wherein the duration of the convergence time is programmable.*"

Applicants further note that there are additional elements recited in amended claim 1 of the present application which are nowhere taught or suggested by Simmonds et al. For example, amended claim 1 of the present application recites "... a signal generating means for receiving the master sync signal and *generating a video clock signal from the master sync signal wherein the video clock signal is synchronized with the master sync signal...*".

Simmonds et al. discloses *either* (i) *generating a clock signal, or* (ii) *receiving an external reference signal and passing that signal through the sync card*, wherein (iii) the clock signal or the master sync signal may be selected via a MUX; but nowhere does

Simmonds et al. teach or suggest that the clock signal is generated from the external reference signal, or that the clock signal may be synchronized with an external clock signal.

Further, Applicants respectfully submit that Simmonds et al. actually *teaches away* from any interaction between, combining of, or synchronization between the external clock and the internal clock. See for example Simmonds et al., column 7, lines 50-62:

> "*The multiplexer 122 selects either the internal reference clock* generated by the internal reference clock oscillator 120 *or the external reference clock input 104.* In particular, *where the sync card is a master sync card, the multiplexer 122 outputs the reference clock generated by the internal reference clock oscillator 120 and ignores the external reference clock input 104.* Alternatively, *where the sync card is a slave sync card, the multiplexer 122 outputs the external reference clock input 104 and ignores the reference clock generated by the internal reference clock oscillator 120.* In other words, each slave sync card ignores the output from its own reference clock oscillator and, instead, uses the reference clock input as the reference clock source as provided by the master sync card."

For the reasons cited above, Applicants respectfully submit that Simmonds, et. al., does not anticipate *amended* claim 1 because it does not teach or suggest each and every feature of that claim. New dependent claims 14-27 are likewise not anticipated by Simmonds et al. for the same reasons as claim 1 from which they depend and further in view of their own respective features. Dependent claims 2 and 6 have been cancelled, thereby rendering the rejections of those claims moot. Accordingly, Applicant respectfully requests that the rejection of claim 1 under 35 U.S.C. § 102(e) be reconsidered and withdrawn, and that dependent claims 14-27 be passed to allowance.

Rejections under 35 U.S.C. § 103(a)

Original claims 3-5 and 7-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Simmonds in view of Moyal (US 6,704,381 B1) ("Moyal et al."), and further in view of Miichi et al. (US 5,880,745 Bl) ("Miichi"). For the reasons set forth below, the Applicant respectfully traverses.

Rejection of Claims 3-5, 7-10, and Support of New Dependent Claims

Claims 3-5 and 7-10 have been cancelled. However, Applicants acknowledge that new claims 14-27 may embody combinations of elements substantially similar to those recited in original claims 3-5 and 7-10. Applicants respectfully submit, however, that such combinations are not anticipated by the Simmonds et al. in view of Moyal et al. or further in view of Miichi.

Original claims 3-5 and 7-10 each depend from original claim 1. As noted above, original claim 1 recited "*a phase lock loop circuit having a digital rate controller to control a lock rate of said phase lock loop circuit*". Similarly, claim 1 as currently amended recites "*the signal generating means* [i.e., the phase-locked loop of the present invention] *reestablishes the synchronization between the master sync signal and the clock signal; and wherein the reestablishment of the synchronization occurs over a convergence time, wherein the duration of the convergence time is programmable*".

As also noted above, while Simmonds et al. discloses a phase-locked loop (PLL), the PLL of Simmonds is used to select between an external reference clock and an internal reference clock. The PLL of Simmonds et al. does not *reestablish a synchronization* between a master sync signal and a locally generated clock signal. As

further noted above, Simmonds et al. does not disclose other features of the present invention, as recited in presently amended claim 1. For example, Simmonds et al. does not disclose "... a signal generating means for receiving the master sync signal and *generating a clock signal from the master sync signal wherein the clock signal is synchronized with the master sync signal...*"

Regarding the Moyal et al. patent, what is disclosed therein is a phase-locked loop (PLL) with a configurable frequency acquisition rate. Applicants respectfully note that Moyal et al. provides no teaching or suggestion that a PLL be used as part of a video synchronization system. In particular, Moyal et al. provides no teaching or suggestion to synchronize an internally generated (i.e., locally) video clock signal with an externally generated master synchronization signal. Moyal et al. actually teaches away from such applications by indicating alternative applications for the PLL disclosed therein: "Applications of PLLs in modern computers may require switching between reference clocks..." (see Moyal et al. column 1, lines 53-54). Hence, rather than maintaining synchronization between a locally generated signal and a single external sync signal, as with the present invention, the Moyal et al. PLL is intended to reestablish synchronization when the PLL is *switched* from one external source to another.

As already noted, there is no teaching or suggestion in Simmonds et al. that the PLL disclosed therein is used to synchronize two signals, or to reestablish synchronization between two signals. As such, there is no motivation to combine provided in either Simmonds et al. or Moyal et al.

However, even assuming, *arguendo*, that the PLL of Moyal et al. might be combined with Simmonds et al., Applicants respectfully submit that the combination of

Simmonds et al. and Moyal et al. do not recite the claimed features of the present invention.

The PLL of Simmonds et al. is used only as a means to help a MUX select between an internal clock signal and an external clock signal. The signal generated by the PLL of Simmonds et al. is fed back into the PLL, but it is not used as an output signal, i.e., it is not used as an output video clock signal. Rather, the PLL of Simmonds et al. only uses its LOCK output (indicating whether or not signal lock has been achieved) to control the MUX (see Fig. 5 on page 3 of Simmonds et al). The PLL of Moyal et al., if somehow employed in the Simmonds et al. invention, may still feed a signal LOCK output to a MUX; however, the PLL would not use the external clock signal to generate an output video clock signal, as no such teaching or suggestion is present in Simmonds et al. or Moyal et al.

As such, the combination would not "...[generate] a video clock signal from the master sync signal wherein the video clock signal is synchronized with the master sync signal; wherein if the video clock signal is no longer synchronized with the master sync signal, the signal generating means reestablishes the synchronization between the video clock signal and the master sync signal...", as with the present invention.

Put another way: The PLL of Simmonds et al. is used only for signal *selection*, but *not* for signal *generation* or signal *synchronization* as with the present invention; hence the PLL of Moyal et al. could not provide either signal synchronization or an adjustable synchronization rate to the video system of Simmonds et al.

The Miichi et al. invention, which teaches a liquid crystal projection apparatus, also does not teach or suggest the missing elements.

For the reasons cited above, Applicants respectfully submit that Simmonds, et. al. in view of Moyal et al., and further in view of Miichi et al., does not anticipate *amended* claim 1 because it does not teach or suggest each and every feature of that claim. New dependent claims 14-27 are likewise not anticipated by the same combination for the same reasons as claim 1 from which they depend and further in view of their own respective features.

Applicants note in particular that new dependent claim 14, which depends directly from amended independent claim 1, recites the video input/output module with the PLL and digital rate controller. While Simmonds et al. discloses a display module, and Moyal et al. discloses a PLL with a configurable frequency acquisition rate, these elements, even if combined, do not provide the functionality of the present invention as recited in amended claim 1 (i.e., as discussed above, the combination would not "...[generate] a video clock signal from the master sync signal wherein the video clock signal is synchronized with the master sync signal; wherein if the video clock signal is no longer synchronized with the master sync signal, the signal generating means reestablishes the synchronization between the video clock signal and the master sync signal..."). Further differences between the PLL of Moyal et al. and the PLL of the present invention are discussed below in conjunction with the rejection of original claim 11.

Dependent claims 3-5 and 7-10 have been cancelled, thereby rendering the rejections of those claims moot. Applicants respectfully request that new dependent claims 14-27 be passed to allowance.

Rejection of Claim 11

Regarding original claim 11, the Examiner has stated (page 7 of the OA):

> "... the modified Simmonds as discussed with respect to the rejection of claim 3 teaches an apparatus (Simmonds "sync card 100") for synchronizing to a first digital signal (Simmonds: "reference clock of the master sync card 100A"), generation of a second digital signal (Simmonds: "the reference clock and raster sync signals" that "slave card 100B" transmits) [Simmonds: col. 7 lines 16-22] comprising:"

Applicant's respectfully point out that, as discussed above (i) neither the Simmonds et al. patent nor the Moyal et al. patent provide motivation to combine, and further (ii) if the two inventions were combined, the result would still not produce an apparatus for synchronizing to a first digital signal generation of a second digital signal.

Regarding the specifics of the Examiner's rejection, Applicants respectfully submit that cited elements of the Moyal et al. patent are in fact not analogous in structure or function to the Applicants' invention as recited in claim 11.

Regarding the last paragraph on page 7 of the Office Action: The phase detector 304 of the present invention compares the first digital signal (the master pulse stream 303) to a comparison pulse stream (the slave pulse stream 305) received from the digital rate controller circuit 314. As recited in claim 11, the comparison pulse stream is produced by dividing the second digital signal by a divisor, "...wherein said digital rate controller produces said divisor value based on a programmable rate value and a comparison of the first digital signal and said comparison pulse stream".

The phase detector disclosed in Moyal et al. compares the first digital signal to a second pulse stream, and may divide the second digital signal by a divisor; but nowhere is there disclosed a "... divisor value based on a programmable rate value and a

comparison of the first digital signal and said comparison pulse stream". In fact, nowhere does Moyal et al. disclose specific means for establishing the divisor value used by the Moyal et al. divider.

As noted by the Examiner on page 8 of the Office Action, third paragraph, Moyal et al. discloses "settings of the feedback divider", Moyal et al., column 5, line 15. Applicants respectfully submit that this does not constitute a teaching or suggestion that a specific synchronization rate value may be programmed into the Moyal et al. divider, nor that a programmable rate value is combined with a comparison of the first digital signal and the second digital signal to produce a divisor value.

The full text cited by the Examiner is Moyal, column 5, lines 11-15, which reads: "The reference pulses REF_UP and REF_DN may be, in one example, (i) set at a predetermined width, (ii) set in response to the voltage control signal from the charge pump/loop filter 54, or (iii) set in response to the settings of the feedback divider 58." Hence, Moyal et al. discloses setting a width for references pulses via "settings" of the divider, not setting a divider value. (Applicants note that nowhere does Moyal et al. further define or clarify the specific nature of the "settings" of the divider.)

There are significant other respects in which the architecture and operation of the Moyal et al. PLL are not analogous to the architecture or operation of the PLL as taught and claimed in the present application. However, Applicants believe the above cited disparities between Moyal et al. and the present application establish that Moyal et al. does not teach or suggest each and every feature of the PLL as recited in claim 11 of the present invention. Neither Simmonds et al. nor Miichi teach or suggest the missing elements.

For the reasons cited above, Applicants respectfully submit that Simmonds, et. al. in view of Moyal et al., and further in view of Miichi et al., does not render claim 11 obvious because it does not teach or suggest each and every feature of that claim. Accordingly, Applicants respectfully request that the rejection of claim 11 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Rejections of Claim 12 and 13

Regarding original claim 12, the Examiner has stated (page 8 of the Office Action):

> " As to claim 12, the modified Simmonds [Simmonds: fig. 3] teaches a system for synchronizing video frame rate between a first video system (Simmonds: "PC 50B") displaying video images on a first display device and a second video system (Simmonds: "PC 50C") displaying video images on a second display device [abstract lines 1-8], the system comprising:
> a master sync signal generator (Simmonds: "sync card 100A"):
> a first video input/output module ("sync card 1008") associated with said first video system; and
> a second video input/output module ("sync card 1000") associated with said second video system,
> All of the claim limitations regarding the components included in said video input/output modules ("sync card 100B" and "sync card 1000") have already been discussed with respect to the rejection of claim 3."

Applicant's respectfully point out that, as discussed above (i) neither the Simmonds et al. patent nor the Moyal et al. patent provide motivation to combine, and further (ii) if the two inventions were combined, the result would still not produce a system as recited in claim 12 for synchronizing the video frame rate between a first video system and a second video system.

In particular, Applicants call attention to the element of claim 12 which recites: "... a voltage controlled oscillator that produces a video clock signal in response to said

analog signal...". The voltage controlled oscillator (VCO) is the final stage of the PLL discussed above, and the video clock signal produced by the VCO is the "... video clock signal [generated] from the master sync signal wherein the video clock signal is synchronized with the master sync signal...."

As discussed above: (i) Simmonds et al. neither teaches nor suggests a method or system for generating a video clock signal that is synchronized with a master sync signal, but instead only teaches a system for selecting either one of a locally generated video signal or a master-video signal; (ii) Even assuming, *arguendo*, a motivation to combine Simmonds et al. with Moyal et al., the combination does not result in the recited element of the system of claim 12 (since the PLL of Simmonds et al. is used only for signal *selection*, but *not* for signal *generation* or signal *synchronization* as with the present invention).

Applicants further call attention to the element of claim 12 which recites "... a digital rate controller that divides said clock signal by a divisor value to produce said slave pulse stream, said digital rate controller producing said divisor value based on a programmable rate value and a comparison of said master pulse stream and said slave pulse stream". As discussed above, the PLL of Moyal et al. does not disclose the recited feature (i.e., a digital rate controller which embodies a digital comparator, a rate controller, and a programmable divider functioning in the claimed manner). Hence, even assuming, *arguendo*, a motivation to combine Simmonds et al. with Moyal et al., the combination does not result in the recited element of the system of claim 12.

Miichi does not teach or suggest the missing elements. For the reasons cited above, Applicants respectfully submit that Simmonds, et. al. in view of Moyal et al., and

further in view of Miichi et al., does not anticipate claim 12 because it does not teach or suggest each and every feature of that claim.

Dependent claim 13 is likewise not anticipated by Simmonds, et. al. in view of Moyal et al., and further in view of Miichi et al., for the same reasons as claim 12 from which it depends, and further in view of its own respective features. Accordingly, Applicant respectfully requests that the rejection of claims 12 and 13 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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